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| **4.** | Consider the sequence of machine instructions given below:  MUL R5, R0, R1  DIV R6, R2, R3  ADD R7, R5, R6  SUB R8, R7, R4  In the above sequence, R0 to R8 are general purpose registers. In the instructions shown, the first register stores the result of the operation performed on the second and the third registers. This sequence of instructions is to be executed in a pipelined instruction processor with the following 4 stages: (1) Instruction Fetch and Decode (IF), (2) Operand Fetch (OF), (3) Perform Operation (PO) and (4) Write back the Result (WB). The IF, OF and WB stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD or SUB instruction, 3 clock cycles for MUL instruction and 5 clock cycles for DIV instruction. The pipelined processor uses operand forwarding from the PO stage to the OF stage.   1. The number of clock cycles taken for the execution of the above sequence of instructions is? 2. Compute the execution time for pipeline and non-pipeline execution of the above program running on processor which has a cycle time of 10ns. |  |  |
| **5.** | **Solve the following questions:**   1. Assume we have 8GB of word addressable memory with a word size of 64 bits and each refill line of memory stores 16 words. We have a direct-mapped cache with 1024 refill lines. Answer the following questions. 2. What is the address format for the cache? 3. If we changed the cache to a 2-way set associative cache, how does the format change? 4. If we changed the cache to a fully associative cache, how does the format change?      1. Consider a memory system that consists of only 12 blocks and there is a 5 blocks cache. The cache is fully associative uses LRU. If a program requires the sequence of blocks shown below   **1 5 4 3 2 8 5 1 4 7 1 7 1 8 4 9**  Calculate the hit ratio and average access time of cache for a memory system consists of a main memory with an access time of 60 nsec and a cache with an access time of 15 nsec. |  |  |